**6t sram**

MNMOS\_1 N\_1 N\_2 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_2 Gnd N\_1 N\_2 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_3 N\_2 wl bl 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_4 blbar wl N\_1 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MPMOS\_1 Vdd N\_1 N\_2 Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_2 N\_1 N\_2 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

**Bit line 9T**

MNMOS\_1 N\_1 rwl N\_2 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_2 wblb wwl N\_3 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_3 N\_2 N\_3 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_4 N\_4 N\_3 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_5 N\_3 N\_4 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_6 N\_4 wwl wbl 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_7 rbl rwl N\_1 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MPMOS\_1 N\_4 N\_3 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_2 N\_3 N\_4 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

**Read stability**

MNMOS\_1 N\_1 N\_2 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_2 N\_3 N\_1 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_3 N\_2 wr bl 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_4 N\_2 ctrl N\_3 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_5 bl N\_3 N\_8 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_6 N\_8 N\_1 blb 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_7 N\_8 rd Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MPMOS\_1 N\_1 N\_2 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_2 N\_3 N\_1 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

**Proposed design**

MNMOS\_1 rd wr bl 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_2 rd N\_1 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_3 N\_1 rd Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_4 N\_2 N\_1 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_5 N\_3 rd N\_2 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_6 blb N\_1 N\_3 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_7 rd ctrl rd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MPMOS\_1 rd N\_1 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_2 N\_1 rd Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

**Array 2 using sense amp(9T)**

MN1 Out A Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MP1 Out A Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MN1 Out1 A 1 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MN2 1 B Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MN3 Out2 Out1 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MP1 Out1 A Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MP2 Out1 B Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MP3 Out2 Out1 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MMN1 Out1 A Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MMN2 Out1 B Gnd 0 NMOS NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MMN3 Out2 Out1 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MMP1 1 B Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MMP2 Out1 A 1 Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MMP3 Out2 Out1 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MNMOS\_1 q1 N\_9 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_2 qbar1 q1 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_3 q1 wl1 N\_1 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_4 N\_25 N\_9 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_5 q1 ctrl1 rd1 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_6 N\_26 rd1 N\_25 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_7 N\_2 N\_9 N\_26 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_11 q0 N\_6 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_13 qbar0 q0 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_14 q0 a0 bl1 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_15 N\_14 N\_6 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_16 q0 ctrl0 rd0 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_17 N\_15 rd0 N\_14 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_18 bl1b N\_6 N\_15 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_21 q N\_3 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_23 qbar q Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_24 q a0 N\_1 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_25 N\_16 N\_3 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_26 q ctrl rd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_27 N\_18 rd N\_16 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_28 N\_2 N\_3 N\_18 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_31 q2 N\_12 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_33 qbar2 q2 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_34 q2 N\_20 bl1 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_35 N\_21 N\_12 Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_36 q2 ctrl2 rd2 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_37 N\_24 rd2 N\_21 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_38 bl1b N\_12 N\_24 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_43 N\_30 Out N\_31 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_44 N\_29 Outb N\_31 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MNMOS\_45 N\_31 sae Gnd 0 NMOS W=70n L=45n AS=7000f PS=340u AD=7000f PD=440u

MPMOS\_10 Out ymux b0 Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_11 N\_29 Outb Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_12 N\_30 Out Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_1 q1 N\_9 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_2 qbar1 q1 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_3 q0 N\_6 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_4 qbar0 q0 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_5 q N\_3 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_6 qbar q Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_7 q2 N\_12 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_8 qbar2 q2 Vdd Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u

MPMOS\_9 Outb ymux bl0b Vdd PMOS W=105n L=45n AS=10500f PS=410u AD=10500f PD=410u